What is claimed is:

[c1] 1. A method for executing machine instructions in a processing device, comprising the steps of:
executing a first instruction;
identifying whether an outcome of the execution of the first instruction satisfies a first specified condition, and setting an accumulative flag result which reflects whether the first instruction satisfies the first specified condition;
executing at least a second additional instruction;
identifying whether an outcome of the execution of the second instruction satisfies a second specified condition, and updating the accumulative flag depending on whether either the first instruction or the second instruction satisfy their respective first and second specified conditions; and
executing a third instruction based on the value of the accumulative flag subsequent to the execution of the first and second instructions.

[c2] 2. The method of claim 1, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand.

[c3] 3. The method of claim 1, wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag
4. The method of claim 1, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand, and wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c4] 5. The method of claim 4, wherein the compare instructions determine whether two respective error conditions are present, and the branch instruction bases it branching determination on whether either of the two respective error conditions are present, as reflected by the value of the accumulative flag after the second compare instruction is performed.

[c5] 6. A computer readable medium containing program code for execution by a processing device, wherein medium includes:
a first instruction for performing a first operation, which, when executed by the processing device, generates a first outcome result;

at least a second additional instruction for performing a second operation, which, when executed by the processing device, generates a second outcome result; and

at least an additional third instruction for performing a third operation based on an accumulative flag, wherein the accumulative flab represents the logical OR of the first and second outcomes.

[c6] 7. The medium of claim 6, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand.

[c7] 8. The medium of claim 6, wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c8] 9. The medium of claim 6, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand, and wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c9] 10. The medium of claim 9, wherein the compare instructions determine whether two respective error conditions are present, and the branch instruction bases it branching determination on whether either of the two respective error conditions are present, as reflected by the value of the accumulative flag after the second compare instruction is performed.

[c10] 11. An apparatus for executing machine instructions, comprising:

a storage for storing an accumulative flag;

logic for executing instructions, and for determining whether the outcomes of the instructions satisfy respective prescribed conditions;

logic for setting the accumulative flag to reflect the outcomes of the instructions, wherein the logic for setting the accumulative flag includes logic for determining the value of the accumulative flag based on the logical OR of at least first and second instructions,

wherein the logic for executing instructions also includes logic for executing at least an additional third instruction based on the value of the accumulative flag stored in the storage.

[c11] 12. The apparatus of claim 11, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand.

[c12] 13. The apparatus of claim 11, wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag

14. The apparatus of claim 11, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand, and wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c13] 15. The apparatus of claim 14, wherein the compare instructions determine whether two respective error conditions are present, and the branch instruction bases it branching determination on whether either of the two respective error conditions are present, as reflected by the value of the accumulative flag after the second compare instruction is performed.

[c14]

16. An apparatus for executing machine instructions, comprising:
a storage for storing an accumulative flag;
logic for executing instructions, and for determining whether the outcomes of the instructions satisfy respective prescribed conditions;
logic for setting the accumulative flag depending on the outcomes of the executed instructions, wherein the logic for setting the accumulative flag includes logic for determining the value of the accumulative flag based on whether at least one instruction within a group of at least two instructions had an outcome which satisfied its respective prescribed condition;
another storage for storing a program that comprises plural instructions, including:
a first instruction for performing a first operation, which, when executed by the processing device, generates a first outcome result;
at least a second additional instruction for performing a second operation, which, when executed by the logic for executing, generates a second outcome result;
at least an additional third instruction for performing a third operation based on

an accumulative flag.

[c15] 17. The apparatus of claim 16, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand.

[c16] 18. The apparatus of claim 16, wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c17] 19. The apparatus of claim 16, wherein the first and second instructions are compare instructions that each compare a first operand with a second operand, and wherein the third instruction is a branch instruction which bases its branching determination on the value of the accumulative flag.

[c18] 20. The apparatus of claim 19, wherein the compare instructions determine whether two respective error conditions are present, and the branch instruction bases it branching determination on whether either of the two respective error conditions are present, as reflected by the value of the accumulative flag after the second compare instruction is performed.